Integrated
Circuit
Systems, Inc.

WaveFront™ Synthesizer

General Description

The WaveFront Synthesizer, **ICS2115**, is an audio synthesis chip which utilizes wavetable lookup to produce 16-bit, CD quality sound. The internal memory management unit allows both ROM, for standard samples, and low cost DRAM, for soft loadable samples, to be connected directly to the **ICS2115**. The WaveFront Synthesizer presents the audio output in 16-bit linear form for conversion by a low cost CD-type DAC.

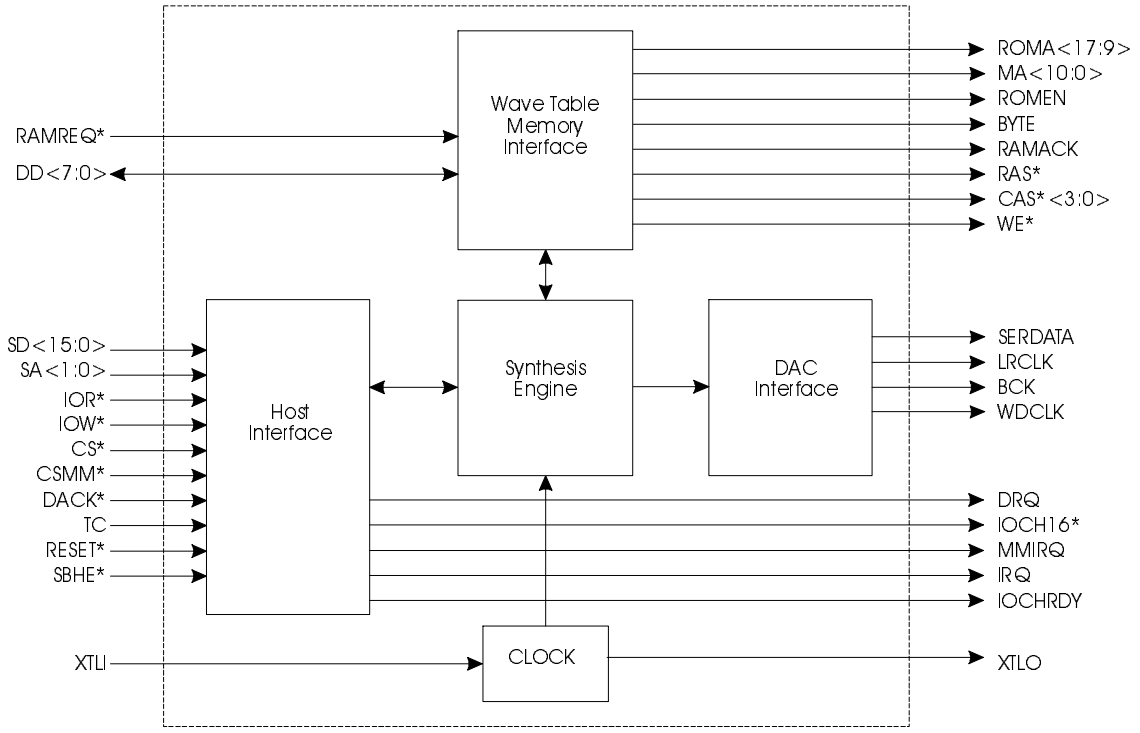
Features

- Capable of addressing up to 32 MB of wavetable ROM and up to 16 MB of wavetable DRAM
- Variable Polyphony Rates: 24 voices at 44.1 kHz through 32 voices at 33.8 kHz
- Uses 16 bit linear, 8 bit linear, and 8 bit u-Law wavetable data
- Serial output for a CD player-type DAC
- Capable of using either a 68EC000 (with the ICS2116) or an ISA-based host for software control
- Part of a complete design package that includes software drivers for Windows and DOS

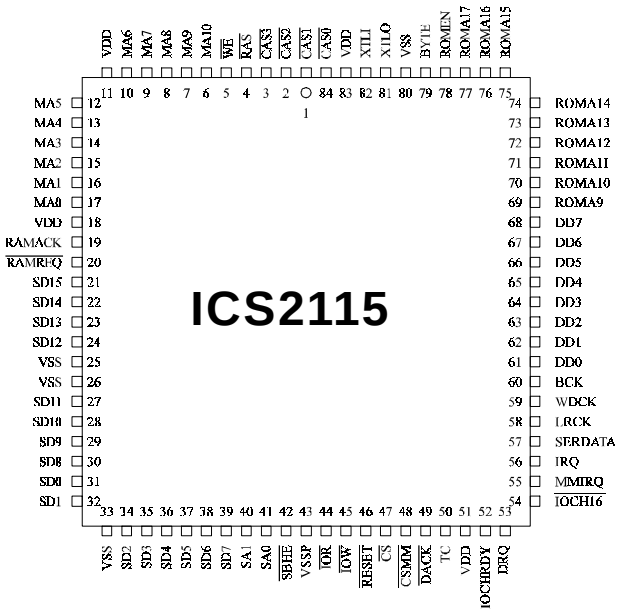
Applications

- ISA based sound cards
- Wavetable synthesizer daughter cards
- External sound modules that connect to a PC's serial or parallel port
- Any system requiring a self contained unit that provides high quality music synthesis of General MIDI sounds, in a low cost design

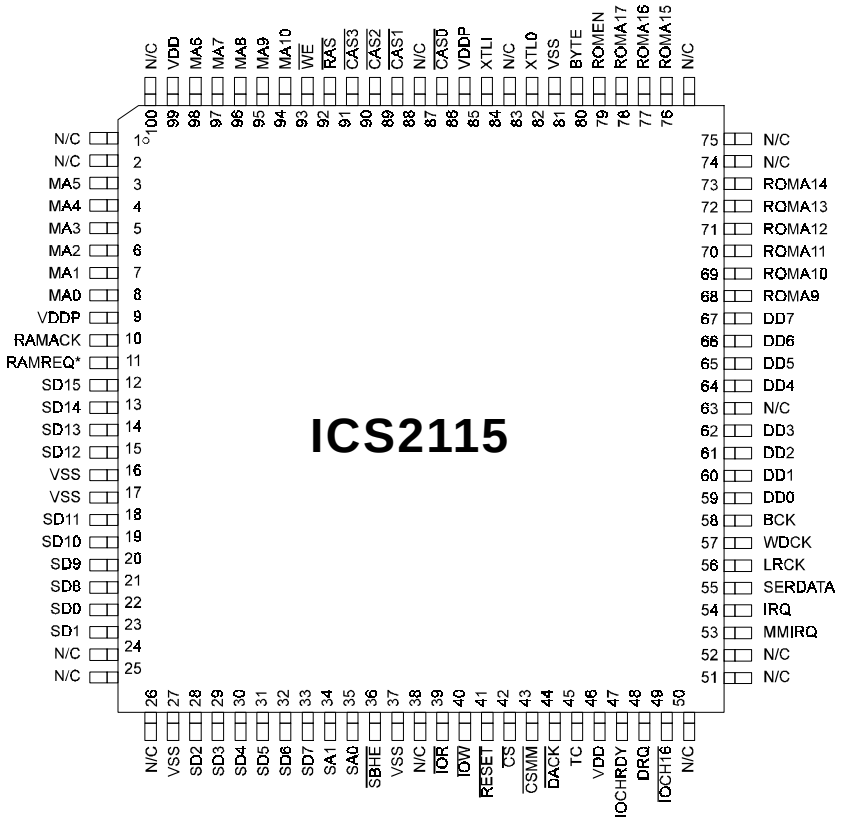
Block Diagram



Pin Configuration



84-Pin PLCC



100-Pin TQFP

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
6-10, 12-17	MA<10:0>	TPUP2	Wavetable Muxed Address Bus.
69-77	ROMA<17:9>	O	Wavetable ROM Address.
1-3, 84	$\overline{\text{CAS}}$<3:0>	O2	Wavetable DRAM Column Address Strobe.
61-68	DD<7:0>	B	Wavetable Data Bus.
4	$\overline{\text{RAS}}$	O2	Wavetable DRAM Row Address Strobe.
5	$\overline{\text{WE}}$	TPUP	Wavetable DRAM Write Enable.
78	ROMEN	O	Wavetable ROM Enable/Byte Enable.
79	BYTE	O	Wavetable ROM Byte Mode.
20	$\overline{\text{RAMREQ}}$	IPUP	Wavetable DRAM cycle request.
19	RAMACK	O	Wavetable DRAM cycle acknowledge.
27-32, 34-39	SD<15:0>	B	Host Interface Data Bus.
40-41	SA<1:0>	I	Host Interface Address Bus.
44	$\overline{\text{IOR}}$	I	Host Interface Read Strobe (Active Low).
45	$\overline{\text{IOW}}$	I	Host Interface Write Strobe (Active Low).
42	$\overline{\text{SBHE}}$	IPUP	Host Interface Sixteen Bit Hardware Enable.
54	$\overline{\text{IOCS16}}$	SINK	Host Interface I/O Channel Sixteen Wide.
47	$\overline{\text{CS}}$	I	Host Interface Synthesizer Chip Enable.
48	$\overline{\text{CSMM}}$	I	Host Interface Chip Select for MIDI Interface Emulation.
53	DRQ	SOURCE	Host Interface DMA Request.
49	$\overline{\text{DACK}}$	I	Host Interface DMA Acknowledge.
50	TC	I	Host Interface DMA Terminal Count.
52	IOCHRDY	SINK	Host Interface I/O Channel Ready.
56	IRQ	B2	Host Interface Synthesizer IRQ.
55	MMIRQ	SOURCE	Host Interface MIDI IRQ.
46	$\overline{\text{RESET}}$	IPUPS	Hardware Reset (Active Low).
57	SERDATA	O	Serial Data Output.
58	LRCK	O	Left/Right Clock.
59	WDCK	O	Word Clock.
60	BCK	O	Bit Clock.
81	XTLO	O (special)	Crystal or N/C.
82	XTL1	I (special)	Crystal or Clock Input.
11, 51	VDD	PWR	Power for chip core.
18, 83	VDDP	PWR	Power for pad ring.
33, 80	VSS	GND	Ground for chip core.
25, 26, 43	VSSP	GND	Ground for pad ring.

Pin Type Descriptions

PIN TYPE	INPUT TYPE	DRIVE	PULLUP R	PULL-DOWN R	NOTES
I	TTL	none	none	none	TTL Input.
IPUP	TTL	none	yes	none	TTL Input with pull-up.
IPUPS	SCHMIDT	none	yes	none	SCHMIDT Input with pull-up.
O	n/a	standard	none	none	Output.
O2	n/a	high	none	none	High Drive Output (200pF max load).
B	TTL	standard	none	none	TTL Bi-directional.
B2	SCHMIDT	standard	none	yes	Drive only with pull-up.
TPUP	n/a	standard	yes	none	Tristate with pull-up.
TPUP2	n/a	medium	yes	none	Tristate (medium drive) with pull-up (125pF max load).
SINK	n/a	standard	yes	none	Drive low only with pull-up.
SOURCE	n/a	standard	none	yes	Drive high only with pull-down.
PWR	n/a	n/a	none	none	Power terminal.
GND	n/a	n/a	none	none	Ground terminal.

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to 7.0V
Logic inputs . . . . . -0.5V to V_{DD} + 0.5V
Ambient operating temp. . . . . 0°C to 70°C
Storage temperature . . . . . -65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Electrical Characteristics

V_{CC} = 5.0V ± 10%; GND = 0V; T_A = 0°C to 70°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.75	5.00	5.25	V
TTL Input Voltage Low	V_{IL}		-0.30		0.80	V
TTL Input Voltage High	V_{IH}		2.20		VDD+0.30	V
Schmidt Input Voltage Low	V_{ILS}		-0.30		1.50	V
Schmidt Input Voltage High	V_{IHS}		3.00		VDD+0.30	V
XTLI Input Voltage Low	V_{ILX}		-0.30		1.50	V
XTLI Input Voltage High	V_{IHX}		3.50		VDD+0.30	V
Output Low Current Standard Drive	I_{OL}	V_{OL}=0.4V	4.0	6.0		mA
Output High Current Standard Drive	I_{OH}	V_{OH}=2.8V		-6.0	-4.0	mA
Output Low Current Medium Drive	I_{OL2}	V_{OH}=0.4V	6.0	9.0		mA
Output High Current Medium Drive	I_{OH2}	V_{OH}=2.8V		-9.0	-6.0	mA
Output Low Current High Drive	I_{OL3}	V_{OH}=0.4V	9.0	12.0		mA
Output High Current High Drive	I_{OH3}	V_{OH}=2.8V		-12.0	-9.0	mA
Input Leakage Current Standard Inputs	I_{IN}	VSS < V_{IN} < VDD	-1.0		1.0	uA
Pull-up Current	I_{PUP}	V_{IN} = VSS	15.0	30.0	50.0	uA
Pull-down Current	I_{PDN}	V_{IN} = VDD	50.0	90.0	150.0	uA
XTLI Input/ Output Capacitance	C_{XTL}			20.0		pF

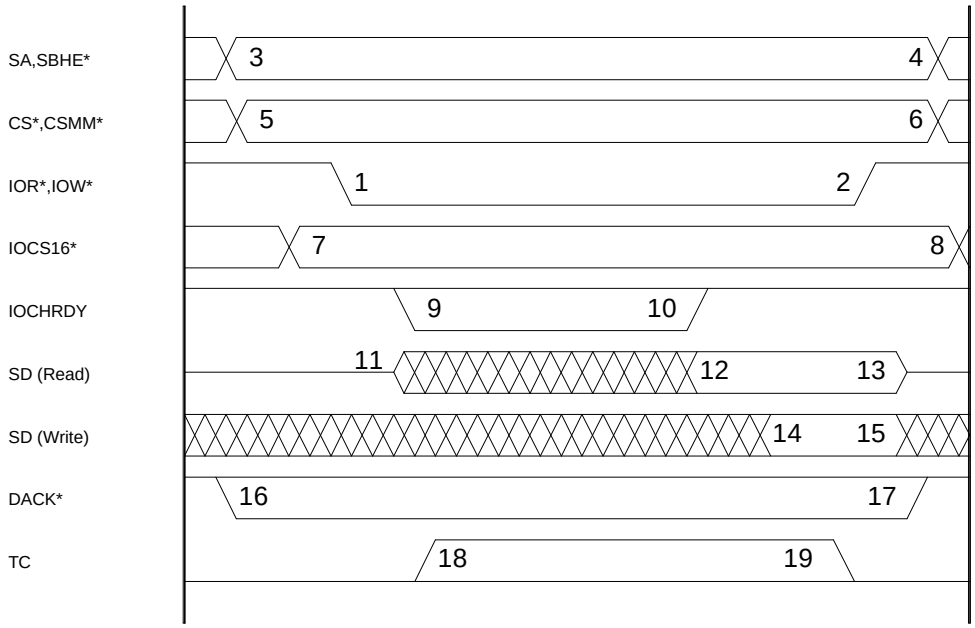
Note: All pins have a maximum capacitive load of 50pF unless noted otherwise.

AC Electrical Characteristics

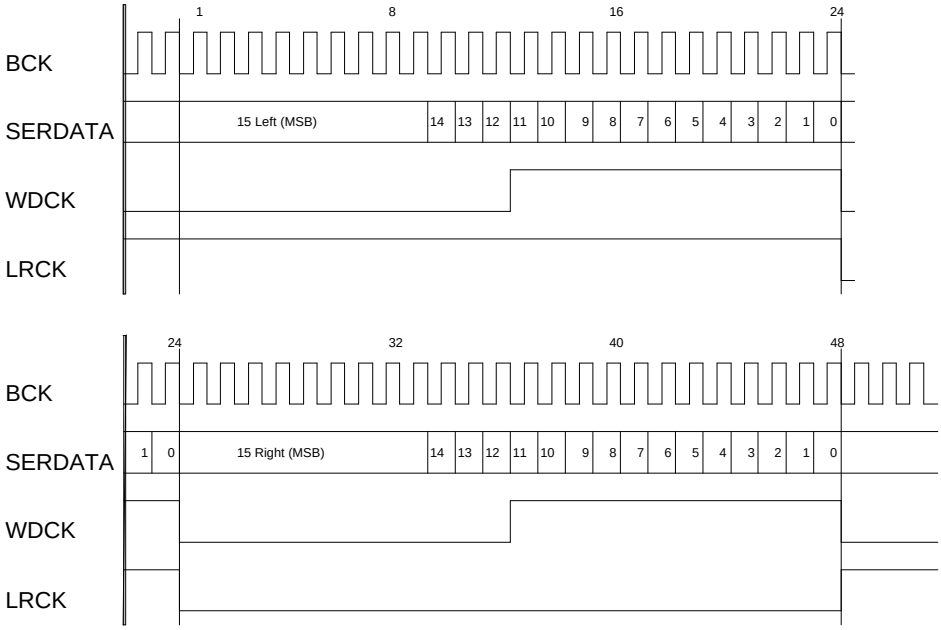
Please reference the timing diagram titled *Host Interface Timing*, below.

HOST INTERFACE AC TIMING PARAMETERS						
PARAMETER	SYMBOL	FROM	TO	MIN	MAX	UNITS
Address setup to command	t_{AS}	3	1	10	-	nS
Chip select setup to command	t_{CS}	5	1	10	-	nS
Address hold from command	t_{AH}	2	4	10	-	nS
Chip select hold from command	t_{CH}	2	6	10	-	nS
Command width	t_{CW}	1	2	100	-	ns
Address valid to /IOCS16 delay	t_{AID}	3, 5	7	0	50	nS
$\overline{\text{IOCS16}}$ hold from address invalid	t_{IH}	4, 6	8	0	50	nS
Write data setup	t_{DS}	14	2	50	-	nS
Write data hold	t_{DHW}	2	15	10	-	nS
Read data delay (ready access)	t_{DD}	1	12	0	60	nS
Read data hold	t_{DHR}	2	13	0	20	nS
$\overline{\text{DACK}}$ setup to command	t_{DAS}	16	1	20	-	nS
$\overline{\text{DACK}}$ hold after command	t_{DAH}	2	17	50	-	nS
TC setup to command	t_{TS}	18	2	25	-	nS
TC hold after command	t_{TH}	2	19	n/a	-	nS
TC width	t_{TW}	18	19	20	-	nS

Timing Diagrams

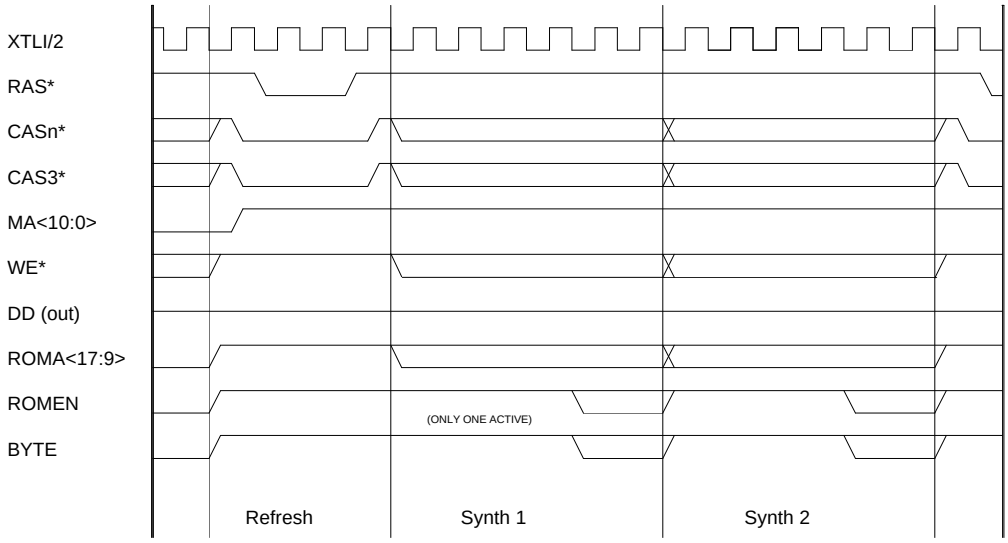


Host Interface Timing

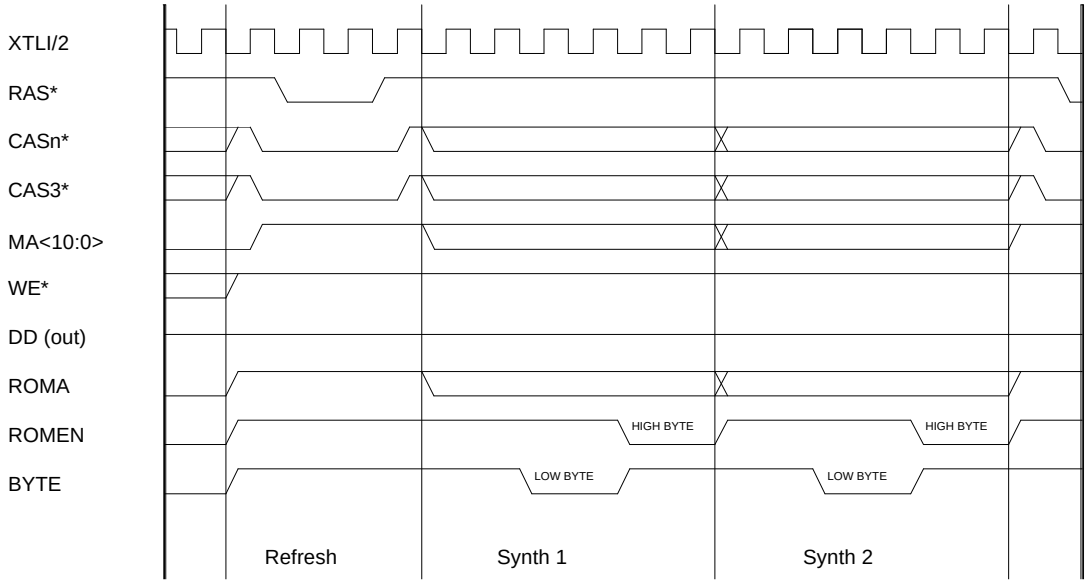


Notes:
- BCK is XTLI frequency divided by four
- 'Extra' cycles are appended as needed for the number of voices
- BCK continues to run for all 'extra' cycles

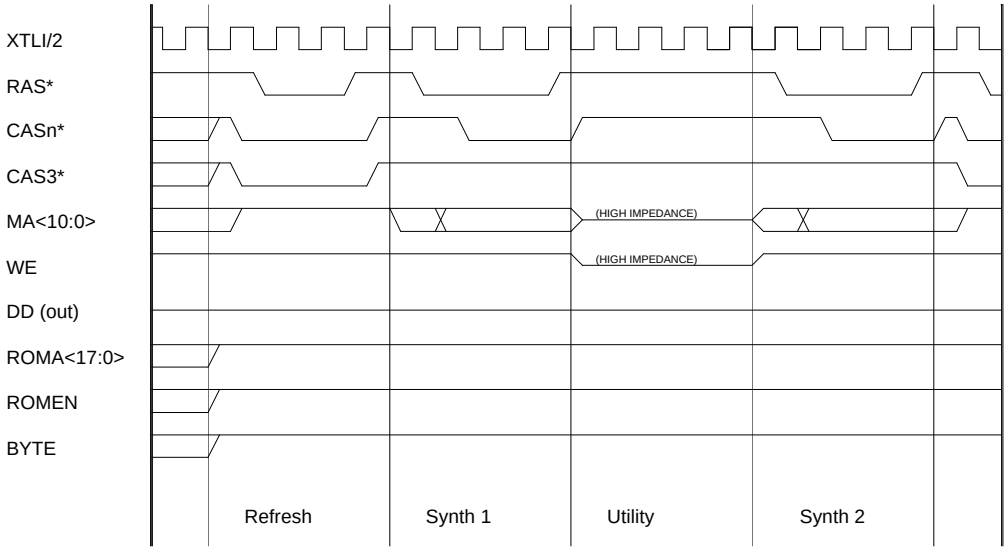
DAC Output Timing



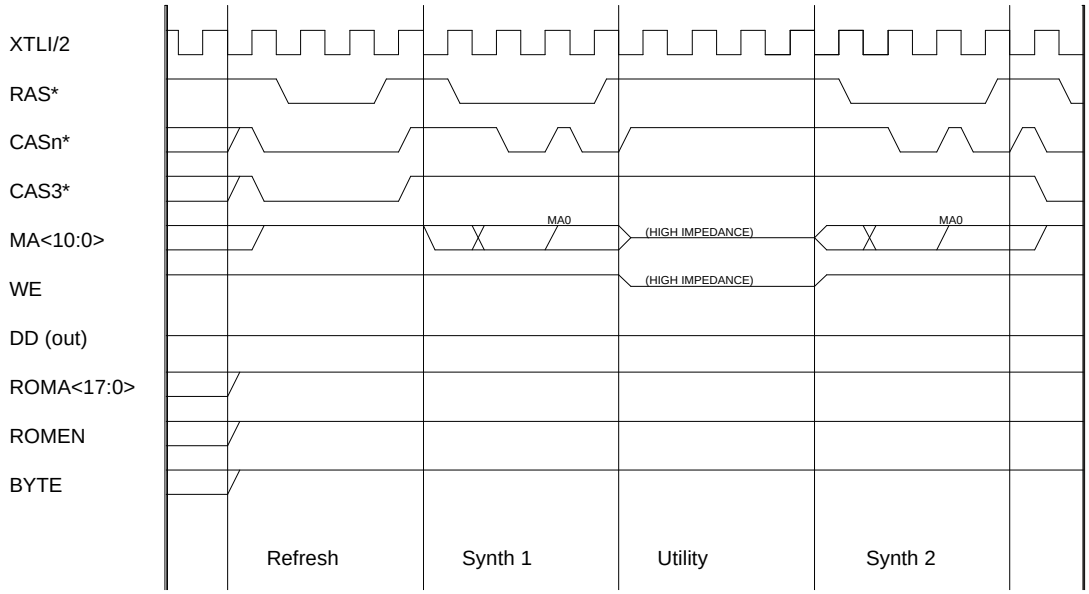
8 Bit/u-Law Access of Wavetable ROM



16 Bit Access of Wavetable ROM



8 Blt/u-Law Access of Wavetable DRAM



16 Bit Access of Wavetable DRAM

Miscellaneous Pins

VDD, VDDP
These are the chip power supply pins. VDD pins power the core logic, while VDDP pins power the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip. These pins MUST be at the same potential externally.

VSS, VSSP
These are the chip ground pins. VSS pins ground the core logic, while VSSP pins ground the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip. These pins MUST be at the same potential externally.

XTLI, XTLO
These pins comprise a self-contained oscillator circuit for primary chip clock generation. No external components (other than the crystal itself) are required for fundamental mode operation. There is approximately 20pF of capacitance at each pin, and a DC bias feedback between the pins for startup and biasing. The standard crystal frequency is 33.868800 MHz (for 24 oscillators at 44.1 kHz or 32 oscillators at 33.8 kHz). Due to the expense of fundamental mode crystals of this frequency, the oscillator can be operated in 3rd overtone mode with the addition to the XTLO pin of a series network to ground of a 1.0H inductor and a 0.001F capacitor. In this case, the crystal fundamental frequency will be 11.2896 MHz.

When an external clock is supplied, XTLO should be left floating. XTLI should be connected to the clock source via a series capacitor (0.001uF is recommended). Duty factor is not critical, since the clock is internally divided by two.

Host Interface

The **ICS2115** can interface with the ISA bus or directly with the ICS2116. For more information, refer to the WaveFront Application Notes. (Please reference the timing diagram titled *Host Interface Timing*, above.)

$\overline{CS}$
This input pin selects read/write access to the internal indirect registers, as selected by SA<1:0>. This signal must be stable before, during, and after $\overline{IOR}$ or $\overline{IOW}$ strobes.

$\overline{CSMM}$
This input pin selects read/write access to the Media Master and MIDI interface emulation registers, as selected by SA<1:0>. This signal must be stable before, during, and after $\overline{IOR}$ or $\overline{IOW}$ strobes.

SA<1:0>
These address input pins select one of four direct mapped registers as determined by the $\overline{CS}$ and $\overline{CSMM}$ pins. These signals must be stable before, during, and after $\overline{IOR}$ or $\overline{IOW}$ strobes.

$\overline{SBHE}$
This input pin determines the access width for even addresses, and is ignored for odd addresses. It should be connected directly to the ISA bus for a 16-bit card. For 8-bit cards, it should be tied high.

$\overline{IOCS16}$
This output pin indicates to the host that the current address is accessible as a word-wide (sixteen bit) data entity. It is based on the current value of the indirect register address, SA<1:0>, and $\overline{CS}$ selecting a word-wide internal register. Under these conditions, $\overline{IOCS16}$ drives low; otherwise, it is a resistive high. This output pin is unused with systems that contain the ICS2116. $\overline{IOCS16}$ requires an external pull-up of 3.3K.

SD<15:0>
This is the bi-directional data bus used for all register data transfers.

$\overline{IOR}$
This input pin is used to read registers when low. SA<1:0>, $\overline{CS}$, $\overline{CSMM}$, and $\overline{SBHE}$ must be stable before, during, and after the active low pulse on $\overline{IOR}$.

$\overline{IOW}$
This input pin is used to write registers when low. SA<1:0>, $\overline{CS}$, $\overline{CSMM}$, and $\overline{SBHE}$ must be stable before, during, and after the active low pulse on $\overline{IOW}$. SD<15:0> must be stable before, during, and after the trailing (rising) edge of /IOW.

IOCHRDY
This output pin is normally in a resistive pull-up state. During $\overline{IOR}$ or $\overline{IOW}$ low times, this pin can become active (drive low) to indicate to the host that the requested data transfer is not ready, and that $\overline{IOR}$ or $\overline{IOW}$ should be held (stretched) until ready is signaled by IOCHRDY deactivating (resistive high). IOCHRDY requires an external pull-up of 3.3K.

$\overline{DACK}$
This input, when low, identifies the current IO operation as a DMA acknowledge operation. The current IO operation will interact with the DMA control logic in the **ICS2115** as programmed, and cause DRQ to be de-asserted. This input must be held before, during, and after the IO command signal ($\overline{IOR}$ or $\overline{IOW}$ low).

TC
This input (along with $\overline{DACK}$ being low) signals that the current DMA operation is the last transfer, and that the **ICS2115** should shutdown its DMA logic after the current transfer is complete.

DRQ
This output pin is normally in a resistive low state. When DMA operation has been programmed and the proper status exists, the DRQ pin will drive high to indicate that the **ICS2115** is ready to accept a DMA data transfer. Upon receipt of a low on the $\overline{DACK}$ input, DRQ will return to the resistive low state. When the **ICS2115** is ready to continue DMA transfers, DRQ will again be asserted. This sequence repeats until DMA is terminated by either TC or a register write. DRQ requires an external pull-down of 1K.

MMIRQ
This output is normally in a resistive low state. Whenever an active *Media Master* interrupt occurs, it will drive high. When the interrupt condition is cleared, the pin returns to a resistive low state. MMIRQ requires an external pull-down of 1K.

IRQ
This output is normally in a resistive low state. Whenever an active internal interrupt occurs, it will drive high. When the interrupt condition is cleared, the pin returns to a resistive low state. IRQ requires an external pull-down of 1K.

$\overline{RESET}$
This input is the active low hardware reset for the **ICS2115**.

DAC Output

The **ICS2115** is designed to directly interface with consumer CD player type digital to analog converters. The interface is a 48 clock, MSB first, left/right multiplexed data stream. Depending on the number of oscillators enabled, there will be additional idle clocks generated after the data is output. (Please reference the timing diagram titled *DAC Output Timing*, above.)

Some DACs that may be used are:

- Phillips TDA1545
- NEC UDP6376

BCK
This output pin is the bit clock for the DAC. The frequency of BCK is the frequency of XTLI divided by four. It always runs, even when the system has not initialized itself. The other DAC interface signals change on the falling edge of BCK, and are stable on the rising edge of BCK.

SERDATA
This output is the accumulated data of all **ICS2115** oscillators, presented as signed binary two's complement data, MSB first. The internal 16 bit data is sign-extended to 24 bits, and presented left then right.

LRCK
LRCK indicates the stereo channel of the data just shifted out. It will transition high to low after bit 0 of the left data has been output, and transition low to high after bit 0 of the right data has been output.

WDCK
WDCK indicates the framing of the data being shifted out. It will transition low to high between bits 12 and 11 of both the left and right data words. It transitions high to low after bit 0 of both the left and right data words.

Wavetable Memory Interface

(Please reference the timing diagrams that show the wavetable memory access cycles, above.) The **ICS2115** is designed to directly interface to the following memory components:

- dynamic RAM meeting the following parameters:
  - 80nS access time
  - Fast Page mode operations
  - CAS-before-RAS auto-refresh
  - 256K (9 addresses) to 4M (11 addresses) by 1 or 4 (configured as byte wide)

SIMM's with an access time better than 80ns can also be used.

- ROM meeting the following parameters:
  - 150nS address access time
  - 70nS output enable access times
  - byte-wide output

The ICS2122-001, ICS2124-001 and ICS2124-002 comprise the ICS 2 MB and 4 MB patch sets respectively. Users of the WaveFront chipset can either buy ROMs directly from ICS or purchase the mask and produce the wavetable ROMs independently.

Pin descriptions follow.

DD<7:0>
This bus is a bi-directional data bus for the wavetable data. It functions as an input under all operations except for DMA writes to DRAM. This bus connects directly to the data pins of all wavetable DRAM and ROM.

MA<10:0>
This output bus drives addresses to both DRAM and ROM wavetable memory.

$\overline{CAS}$*<3:0>*
These outputs function as both $\overline{CAS}$ inputs to up to four banks of DRAM and as addresses to ROM. For a DRAM cycle, only one of these four outputs will toggle active (low) at a time. For a refresh cycle, they all toggle low to refresh all DRAM simultaneously.

$\overline{RAS}$
This output connects to the $\overline{RAS}$ pin of all wavetable DRAM chips $\overline{RAS}$ is generated for all DRAM access and refresh cycles, and remains high for all ROM cycles so that the /CAS pins can be used as ROM addresses.

$\overline{WE}$
This tristate output connects to the $\overline{WE}$ pin of all wavetable DRAM. It is normally in a driven (or resistive) high state. It toggles low only for DMA write cycles.

ROMA<17:9>
This bus provides addresses for ROM based oscillators. During refresh and DRAM cycles, these pins are driven high. The MA<10:0> and CAS<3:0> multiplex to provide the other address bits for the wavetable ROM. The table below shows the exact relation.

Wavetable ROM address	ICS2115 Signal
A0	MA<0>
A1	MA<1>
A2	MA<2>
A3	MA<3>
A4	MA<4>
A5	MA<5>
A6	MA<6>
A7	MA<7>
A8	MA<8>
A9	RA<9>
A10	RA<10>
A11	RA<11>
A12	RA<12>
A13	RA<13>
A14	RA<14>
A15	RA<15>
A16	RA<16>
A17	RA<17>
A18	$\overline{CAS}$<3>
A19	MA<9>
A20	MA<10>
A21	$\overline{CAS}$<0>
A22	$\overline{CAS}$<1>
A23	$\overline{CAS}$<2>

BYTE
BYTE functions as Low Byte $\overline{OE}$ for the low byte ROM of a 16-bit ROM pair. When using the ICS2122-001, this connects to the output enable on the ROM. When using the 4 MB patch set, BYTE connects to the $\overline{OE}$ on the ICS2124-001.

ROMEN
ROMEN functions as High Byte $\overline{OE}$ for the high byte ROM of a 16-bit ROM pair. For systems using the ICS2122-001, this pin is unused. When using the 4 MB patch set, ROMEN connects to the $\overline{OE}$ on the ICS2124-002.

$\overline{RAMREQ}$
This input pin is used to request an external memory cycle. Its function is unused in the present design. $\overline{RAMREQ}$ should be tied high.

RAMACK
This output pin provides acknowledgment of an external memory cycle. It is unused in the current design.

MPU-401/6850 Emulation Registers

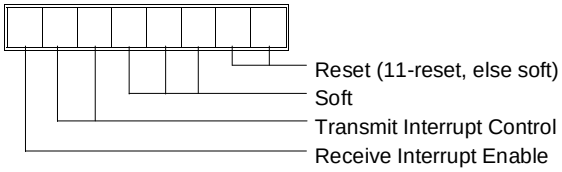
These 4 registers will be mapped at an offset determined by the $\overline{CSMM}$ input. The WaveFront Synthesizer only decodes the least significant 2 address bits. For identification purposes, this document refers to these registers as Emulation Base + 0 through Emulation Base + 3.

MIDI Emulation Control/Status Register

The MIDI Control Status register can be configured as either a 6850 compatible or an MPU-401 compatible UART. The WaveFront Operating System writes to the IndEmulMode Register to indicate the mode of emulation.

6850 Mode Control (Emulation Base + 0) (Write Only)

The host can access this MIDI control register by writing to this address. The control register is mapped as follows.

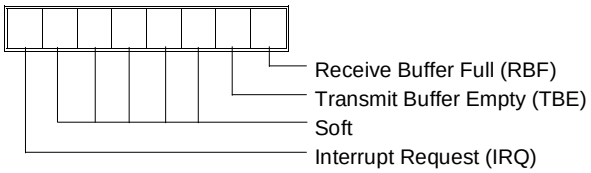


MIDI (6850) Control Register

1:0 - Reset - Resets the MIDI Port
  11 = Reset (Resets Receive Interrupt and Receive Interrupt Enable)
  00, 01 and 10 = No Reset
4:2 - Soft - Software controlled functions
6:5 - Transmit Buffer Empty Interrupt Control
  01 = Interrupts are enabled
  00, 10 and 11 = Interrupts disabled
7: - Receive Buffer Full Interrupt Enable
  1 = Interrupts enabled
  0 = Interrupts disabled

6850 Mode Status (Emulation Base + 0) (Read Only)

The host can access this MIDI status register by reading this address. The status register is mapped as follows.

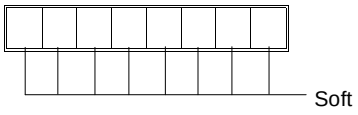


MIDI (6850) Status Register

0: - Receive Buffer Full
  1 = full
  0 = empty
1: - Transmit Buffer Empty
  1 = empty
  0 = full
6:2 - Soft
7: - Interrupt Request
  1 = Interrupt pending
  0 = Interrupt not pending

MPU-401 Mode Control (Emulation Base + 1) (Write Only)

The host can access this MIDI control register by writing to this address. The control register mapping is software dependent.

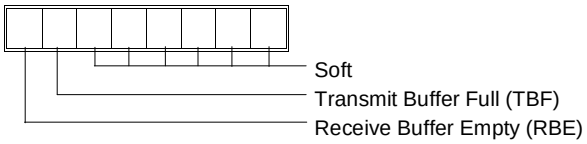


MIDI (MPU-401) Control Register

7:0 - Soft - Software controlled functions

MPU-401 Mode Status (Emulation Base + 1) (Read Only)

The host can access this MIDI status register by reading this address. The status register is mapped as follows.



MIDI (MPU-401) Status Register

5:0 - Soft
6: - Transmit Buffer Full
1 = full
0 = empty
7: - Receive Buffer Empty
1 = empty
0 = full

MIDI Emulation Data Register

This register is the MIDI data port for writing and reading MIDI data. The host can transfer MIDI data between itself and the WaveFront Operating System via this register.

6850 Mode Data (Emulation Base + 1) (Read/Write)

Eight bit data.

MPU-401 Mode Data (Emulation Base + 0) (Read/Write)

Eight Bit data

Registers Emulation Base + 2 and Emulation Base + 3

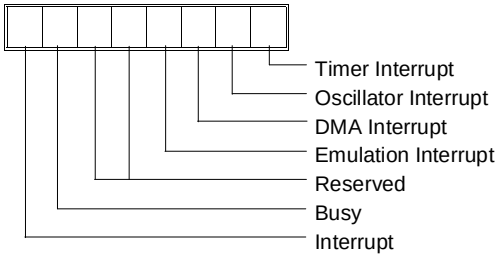
These registers are reserved when the **ICS2115** is in the host configuration

Synthesizer Registers

In the **ICS2115**, the Synthesis and General Purpose registers are accessed indirectly via the Indirect I/O Registers. These 4 registers will be mapped at an offset determined by the $\overline{CS}$ input. For identification, this document refers to these registers as Synthesizer Base + 0 through Synthesizer Base + 3.

Synthesizer Base + 0	R	IRQ/Status
Synthesizer Base + 1	R/W	Register Address
Synthesizer Base + 2	R/W	Data Low Byte/Word
Synthesizer Base + 3	R/W	Data High Byte/Byte

Interrupt status (Synthesizer Base + 0) Read Only



Interrupt Status Register

Note: Reading this Register does NOT clear any of the bits.
0: - Timer Interrupt
This indicates that one or both of the 2 internal WaveFront timers has expired.
1: - Oscillator Interrupt
When this interrupt occurs the WaveFront Operating Systems reads the Oscillator Interrupt Address register to determine the oscillator that needs servicing.
2: - DMA Interrupt
The DMA channel has completed a transfer.
3: - Emulation Interrupt
When this occurs it indicates that a read or write has occurred with one of the High Level Emulation Control or Data registers
4: - Reserved
5: - Reserved
6: - Busy
Status bit which indicates that the previous write operation to an internal register has not yet completed and thus a new write should not be initiated.
7: - Interrupt
This is the Operating System interrupt from the **ICS2115**.

Indirect Register Access

There are two types of indirect registers in the chips; Synthesizer and General Purpose. Due to the timing restrictions on access to the internal indirect registers, access to the two types of registers are handled differently. In **ICS2115**, register addresses $00 through $3F are Synthesizer registers (for both read and write), and all others are for General Purpose use.

General Purpose registers are immediately available for access. Synthesizer registers are internally buffered so that the chip hardware completes the data transfers at the required times.

The WaveFront Operating System can read and write internal Synthesizer registers using 8 or 16 bit reads and writes. Access is accomplished via the 3 indirect registers:

Indirect Address (Synthesizer Base + 1)

This will contain the address of the internal Synthesizer register.

Indirect Data Lo (Synthesizer Base + 2)

Contains the Least significant 8 bits of the data to be written to or read from the internal Synthesizer register addressed by the Indirect Address register.

Indirect Data Hi (Synthesizer Base + 3)

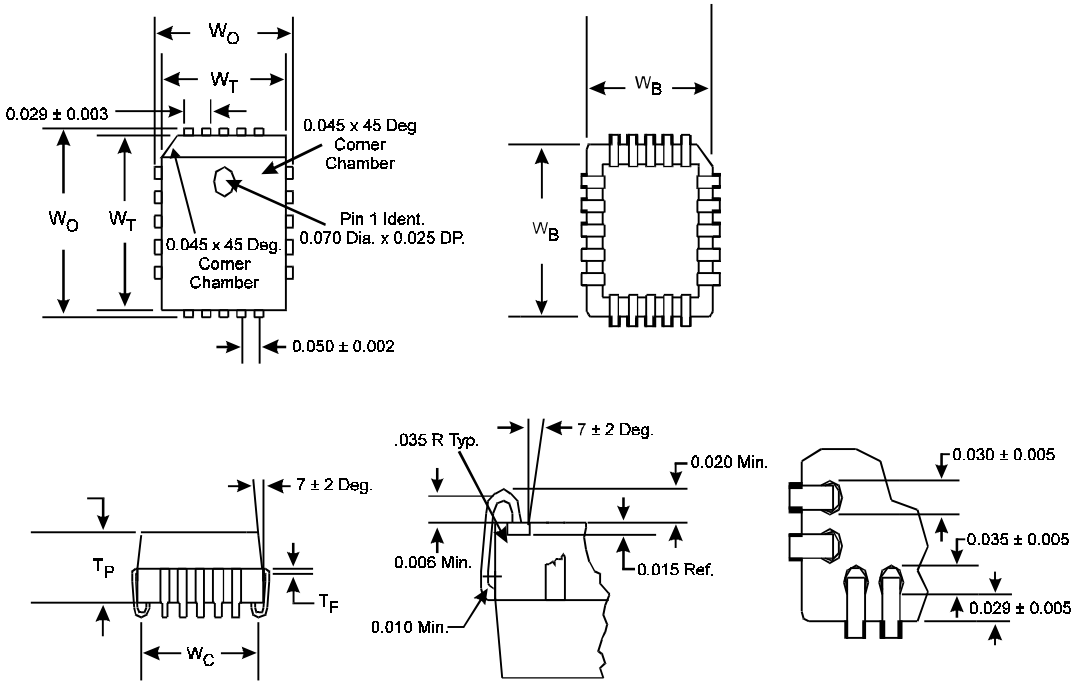
Contains the Most significant 8 bits of the data to be written to or read from the internal Synthesizer register addressed by the Indirect Address register.

Register Map

The following list includes all the internal registers of the **ICS2115** chip and their associated "indirect" addresses. All registers can be read and written unless otherwise indicated.

Synthesizer Register Definitions				
Indirect Address	Rd/Wr	Size	Mnemonic	Description
00	R/W	8	OscConf	Oscillator Configuration
01	R/W	16	OscFC	Wavesample Frequency (6 Integer, 9 Fraction)
02	R/W	16	OscStrtH	Wavesample Loop Start Address (16 Integer)
03	R/W	8	OscStrtL	Wavesample Loop Start Address (4 Integer, 4 Fraction)
04	R/W	16	OscEndH	Wavesample Loop End Address (16 Integer)
05	R/W	8	OscEndL	Wavesample Loop End Address (4 Integer, 4 Fraction)
06	R/W	8	VIncr	Volume Increment
07	R/W	8	VStart	Volume Start Value
08	R/W	8	VEnd	Volume End Value
09	R/W	16	VolAcc	Volume Accumulator
0A	R/W	16	OscAccH	Wavesample Address (16 Integer)
0B	R/W	16	OscAccL	Wavesample Address (4 Integer, 9 Fraction)
0C	R/W	8	OscPan	Pan Value (Note - 10 Bits on 2210)
0D	R/W	8	VCtl	Volume Envelope Control
0E	R/W	8	ActiveOsc	Active Voices
0F	Rd	8	IRQV	Interrupt Source/Oscillator
10	R/W	8	OscCtl	Oscillator Control
11	R/W	8	OscSAddr	Static Address Bits 27-20
12	R/W	8	VMode	Reserved (Write 0)
13-3F	-	X	RESERVED	Do Not Access

General Purpose Register Definitions				
Indirect Address	Rd/Wr	Size	Mnemonic	Description
40	Wr	8	Timer1	Timer Preset 1
41	Wr	8	Timer2	Timer Preset 2
42	Wr	8	Timer1PreS	Prescaler 1
43	R/W	8	Timer2PreS_S	Prescaler 2 (wr) and Timer Status (Rd)
44	Wr	8	DMAddrLo	DMA Start Address Low [11:4]
45	Wr	8	DMAddrMd	DMA Start Address Medium [19:12]
46	Wr	8	DMAddrHi/Data	DMA Start Address high [21:20]
47	R/W	8	DMACS	DMA Control/Status
48	Rd	8	AccMonS	Accumulator Monitor Status
49	Rd	16	AccMonData	Accumulator Monitor Data
4A	R/W	8	DOCIntCS	DOC Interrupt (Read) Int Enable (Write)
4B	Rd	8	IntOscAddr	Address of interrupting Oscillator
4C	R/W	8	MemCfg_Rev	Memory Config. (WR) & Chip Rev. # (Rd)
4D	R/W	8	SysCtrl	System Control
4E	-	X	RESERVED	Do Not Access
4F	R/W	8	OscNumber	Oscillator Address being programmed
50	R/W	8	IndMIDIData	MIDI Data Register
51	R/W	8	IndMIDICS	MIDI Control/Status Register
52	R/W	8	IndHostData	Host Data Register
53	R/W	8	IndHostCS	Host Control/Status Register
54	R/W	8	IndMIDIIntC	MIDI Emulation interrupt Control
55	R/W	8	IndHostIntC	Host Emulation Interrupt Control
56	R/W	8	IndIntStatus	Host/MIDI Emulation Int. Status (Rd)
57	R/W	8	IndEmulMode	Emulation Mode
58-7F	-	X	RESERVED	Do Not Access



LEAD COUNT	FRAME THICKNESS T_F +/-.0003	PKG. THICKNESS T_P +/-.004	PKG. WIDTH TOP W_T +/-.004	PKG. WIDTH BOTTOM W_B +/-.066	OVERALL PKG. WIDTH W_O +/-.005	CONTACT WIDTH W_O +.010/-.030
20L	0.010	0.152	0.350	0.323	0.390	0.320
28L	0.010	0.152	0.450	0.423	0.490	0.420
44L	0.010	0.152	0.650	0.623	0.690	0.620
52L	0.010	0.152	0.750	0.723	0.790	0.720
68L	0.008	0.150	0.950	0.923	0.990	0.920
84L	0.008	0.150	1.160	1.123	1.190	1.120

Ordering Information

ICS2115V

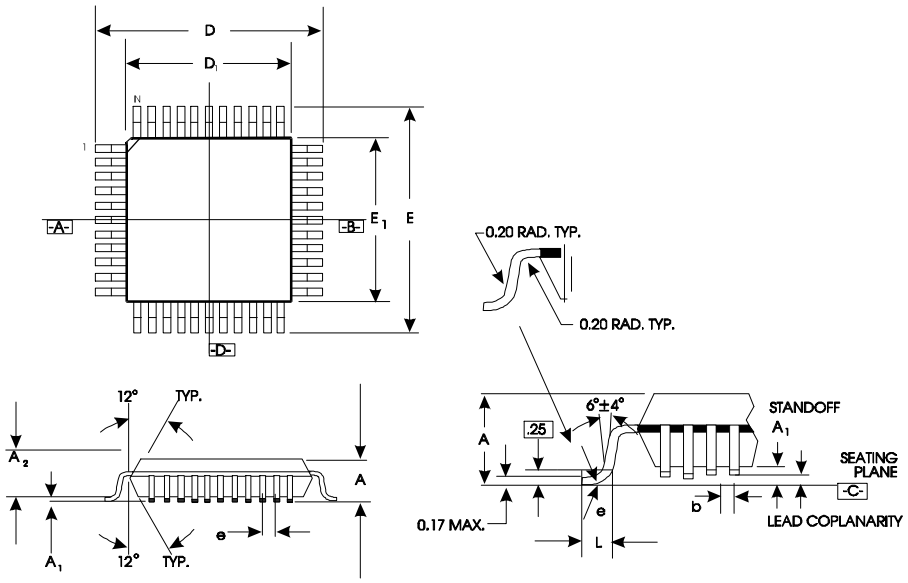
Example:

ICS XXXX M

Package Type
V=PLCC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device



TQFP Package

LEAD COUNT		32L	
BODY THICKNESS		1.00	1.40
FOOTPRINT (BODY+)		2.00	
DIMENSIONS	TOLERANCE		
A	MAX.	1.20	1.60
A_1		0.05 MIN./0.10 MAX.	
A_2	±0.5	1.00	1.40
D	±0.25	9.00	
D_1	±0.10	7.00	
E	±0.25	9.00	
E_1	±0.10	7.00	
L	±0.15/-0.10	0.60	
e	BASIC	0.80	0.50
b	+0.05	0.35	0.22
ccc	MAX.	0.10	0.08
ddd		0.20 MAX.	0.08 MAX.

Ordering Information

ICS2115T

Example:

ICS XXXX M

Package Type
T=TQFP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device